In the Claims:

1-25. (canceled)

26. (new) A processor system comprising:

A. first processor circuitry having a memory transaction bus, a wait signal input, and status signal inputs;

B. second processor circuitry having a memory transaction bus, a wait release signal output, and status signal outputs connected with the status signal inputs;

C. memory circuitry having first connections with the memory transaction bus of the first processor separate from second connections with the memory transaction bus of the second processor circuitry; and

D. wait circuitry having memory transaction bus inputs connected with the memory transaction bus of the first processor circuitry and the first connections, being free of any connections with the memory transaction bus of the second processor circuitry, and having a wait signal output connected with the wait signal input, and a wait release signal input connected with the wait release signal output.

27. (new) The system of claim 26 in which the first processor circuitry includes a system interrupt input, and the wait circuitry has a processor interrupt output coupled with the system interrupt input.

28. (new) The system of claim 26 in which the first processor circuitry has a system interrupt detect output, and the wait circuitry has a system interrupt detect input coupled with the system interrupt detect output.

29. (new) The system of claim 26 in which the first processor circuitry includes a system interrupt input, the wait circuitry has a processor interrupt output and a system interrupt detect input, and including a system interrupt controller having system interrupt output connected with the system interrupt input, a system interrupt detect output connected with the system interrupt detect input, and a processor interrupt input connected with the processor interrupt output.

30. (new) Wait circuitry comprising:

A. first processor interface circuitry having a wait signal output, a processor interrupt output, and memory transaction bus connections;

B. second processor interface circuitry having a wait release signal input and being free of any connections with any memory transaction bus of the second processor circuitry;

C. system interrupt interface circuitry having a system interrupt detect input;

D. decode logic circuitry coupled with the first processor interface circuitry; and

E. control logic circuitry coupled with the first processor interface circuitry, the second processor interface circuitry, the system interrupt interface circuitry, and the decode logic circuitry.